1 – 32. (canceled).

33. (currently amended) A bipolar transistor, comprising:

a collector region;

a base region formed in a base layer overlying the collector region;

an emitter-base dielectric stack overlying the base layer and having an opening therein exposing a portion of the base layer, the emitter-base dielectric stack comprising a carbide layer;

an oxide layer resistive to a carbide-dry-etching process, overlying the carbide layer; and

an emitter poly layer overlying the emitter-base dielectric stack and an exposed portion of the base layer.

34. (currently amended) The transistor of claim 33, wherein the emitter-base dielectric stack comprises:

a first oxide layer overlying the base region of the base layer; and

[a] the carbide layer overlying the first oxide layer.~~; and~~

~~a second oxide layer overlying the carbide layer~~.

35. (currently amended) The transistor of claim 34, wherein the first oxide layer comprises:

a thermal silicon oxide layer overlying the base layer and having a thickness ~~of~~ between about 20 Å ~~or more~~ and about 50 Å ~~or less~~; and

a ~~first~~ deposited silicon oxide overlying the thermal silicon oxide layer and having a thickness of about 50 Å.

36. (currently amended) The transistor of claim 34, wherein the first oxide layer comprises a first silicon oxide overlying the base layer and having a thickness between ~~of~~ about 70 Å ~~or more~~ and about 100 Å ~~or less~~.

37. (original) The transistor of claim 34, wherein the carbide layer comprises a silicon carbide layer overlying the first oxide layer.

38. (currently amended) The transistor of claim 37, wherein the thickness of the silicon carbide layer ~~comprises a thickness of~~ is about 100 Å.

39. (currently amended) The transistor of claim 37, wherein the second oxide layer comprises a second silicon oxide overlying the carbide layer and having a thickness between ~~of~~ about 500 Å ~~or more~~ and about 1000 Å ~~or less~~.

40. (new) A bipolar transistor, comprising:

a collector region;

a base region formed in a base layer overlying the collector region; and

an emitter-base dielectric stack overlying the base layer and having an opening therein exposing a portion of the base layer, the emitter-base dielectric stack including

a thermal oxide layer overlying the based layer having a thermal-oxide thickness;

a first deposited oxide layer overlying the thermal oxide layer having a first thickness;

a carbide layer resistive to an oxide-layer-dry-etching process, overlying the first oxide layer, having a carbide-layer thickness;

a second deposited oxide layer, having a favorable dry-etching selectivity with respect to the carbide layer, overlying the carbide layer, having a second thickness;

the carbide-layer thickness sufficient as an etch-stop for the second deposited oxide layer; and

the second deposited-oxide thickness sufficient as a hard-mask for the carbide layer.